"Low Latency Low Complexity Compare and Decode Architecture for LTE Turbo Codes"

Aaquib Javed[1], Vijay L. Agrawal[2]

P.G Student, Electronics and Telecommunication Department, HVPM's College of Engineering and Technology

Amravati, India[1]

Professor, Electronics and Telecommunication Department, HVPM's College of Engineering and Technology

Amravati, India[2]

Abstract: A new architecture for matching the data protected with an error-correcting code (ECC) is presented in this brief to reduce latency and complexity. Based on the fact that the codeword of an ECC is usually represented in a systematic form consisting of the raw data and the parity information generated by encoding, the proposed architecture parallelizes the comparison of the data and that of the parity information. To further reduce the latency and complexity, in addition, a new butterfly-formed weight accumulator (BWA) is proposed for the efficient computation of the Hamming distance. Grounded on the BWA, the proposed architecture examines whether the incoming data matches the stored data if a certain number of erroneous bits are corrected. For a (40, 33) code, the proposed architecture reduces the latency and the hardware complexity by, compared with the most recent implementation. the proposed architecture reduces the latency and the hardware complexity by ~32% and 9%, respectively, compared with the most recent implementation.

Keywords: Reduce the latency, less complexity, High-speed access, Communication Decoding system.

1. INTRODUCTION

Data comparison is widely used in computing systems to perform many operations such as the tag matching in a cache memory and the virtual-to-physical address translation in a translation look a side buffer (TLB). The data comparison usually resides in the critical path of the components that are devised to increase the system performance, e.g., caches and TLBs, whose outputs determine the flow of the succeeding operations in a pipeline. The circuit, therefore, must be designed to have as low latency as possible, or the components will be disqualified from serving as accelerators and the overall performance of the whole system would be severely deteriorated.

As recent computers employ error-correcting codes (ECCs) to protect data and improve reliability, complicated decoding procedure, which must precede the data comparison, elongates the critical path and exacerbates the complexity overhead. Despite the need for sophisticated designs as described, the works that cope with the problem are not widely known in the literature since it has been usually treated within industries for their products. Recently, however, trigered the attraction of more and more attentions from the academic field. The most recent solution for the matching problem is the direct compare method, which encodes the incoming data and then compares it with the retrieved data that has been encoded as well. Therefore, the method eliminates the complex decoding from the critical path. In performing the comparison, the method does not examine whether the retrieved data is exactly the same as the incoming data.

Instead, it checks if the retrieved data resides in the error correctable range of the codeword corresponding to the incoming data. As the checking necessitates an additional circuit to compute the Hamming distance i.e. the numbers of different bits between the two code words, the saturate adder (SA) as a basic building block for calculating the Hamming distance. However, a practical ECC codeword is usually represented in a systematic form in which the data and parity parts are completely separated from each other. In addition, as the SA always forces its output not to be greater than the number of detectable errors by more than one, it contributes to the increase of the entire circuit complexity.
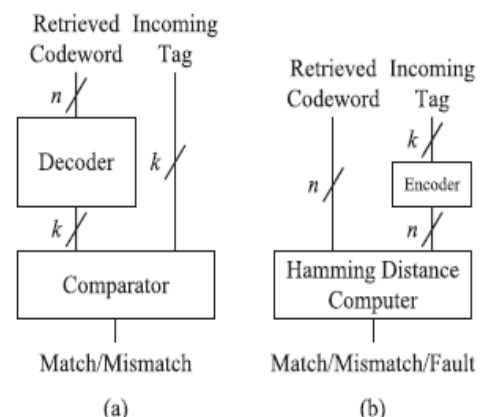

Fig. 1(a) Decode-and-compare architecture and (b) encode-and-compare architecture

2. LITERATURE REVIEW

The decode-and-compare architecture, the n-bit retrieved codeword should first be decoded to extract the original k-bit tag. The extracted k-bit tag is then compared with the k-bit tag field of an incoming address to determine whether the tags are matched or not. As the retrieved codeword should go through the decoder before being compared with the incoming tag, the critical path is too long to be employed in a practical cache system designed for high-speed access. Since the decoder is one of the most complicated processing elements, in addition, the complexity overhead is not negligible. The following section will point out the evolution of the proposed project's work and research till date:

I Performance evaluation of turbo codes using hard decision viterbi algorithm in vhdl

Susrutha Babu Sukhavasi, Suparshya Babu Sukhavasi, Dr.Habibulla Khan, IEEE Chiranjeevi Pilla/ International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 Vol. 2, Issue 3, May-Jun 2012

We first briefly describe the algorithms of convolution encoder and hard decision Viterbi decoder. The focus of this work is towards developing an application specific design methodology for low power solutions. The methodology starts from high level models which can be used for hardware solution and proceeds towards high performance hardware solutions. The methodology starts from algorithmic level, concentrating on the functional correctness rather than on implementation architecture. The effect on performance due to variation in parameters like frame length, number of iterations, type of encoding scheme. Turbo codes are used for error protection, especially in wireless systems.

II Reed-Solomon Turbo Product Codes for Optical Communications: From Code Optimization to Decoder Design

Institut TELECOM, TELECOM Bretagne, CNRS Lab-STICC, Technopˆole Brest-Iroise, CS 83818, 29238 Brest Cedex 3, France Correspondence should be addressed to Rapha¨el Le Bidan Received 31 October 2007; Accepted 22 April 2008

The field of channel coding has undergone major advances for the last twenty years. With the invention of turbo codes followed by the rediscovery of low-density parity check (LDPC) codes, it is now possible to approach the fundamental limit of channel capacity within a few tenths of a decibel over several channel models of practical interest. Although this has been a major step forward, there is still a need for improvement in forward-error correction (FEC), notably in terms of code flexibility, throughput, and cost.

III Turbo and Turbo-Like Codes: Principles and Applications in Telecommunication

K. Gracie is with the Communications Research Centre (CRC) Ottawa, ON K2H 8S2, Canada. M.-H. Hamon is with France Telecom Research and Development, 35512 Cesson- Se´vigne´ Cedex, France Manuscript received August 24, 2006; revised December 20, 2006.

For decades, the de facto standard for forward error correction was a convolution code decoded with the Viterbi algorithm, often concatenated with another code (e.g., a Reed–Solomon code). But since the introduction of turbo codes in 1993, much more powerful codes referred to collectively as turbo and turbo-like codes have eclipsed classical methods. These powerful error-correcting techniques achieve excellent error-rate performance that can closely approach Shannon's channel capacity limit. The lure of these large coding gains has resulted in their incorporation into a widening array of telecommunications standards and systems.

IV Cascaded feed forward architectures for parallel viterbi decoding

G. Fettweis and H. Meyr, "Cascaded feedforward architectures for parallel Viterbi decoding," in Proc. IEEE Int. Sym. Circuits Syst., May 1990, pp. 978–981.

The Viterbi-Algorithm (VA) is a common application of dynamic programming. Since it contains a nonlinear feedback loop (ACS-feedback, ACS: add-compare-select), this loop is the bottleneck in high data rate implementations. In this paper we show that asymptotically the ACS-feedback no longer has to be processed recursively, i.e. there is no feedback, resulting in negligible performance loss. This can be exploited to derive purely feed forward architectures for Viterbi decoding, such that a modular cascadable implementation results. By designing one cascadable module, any speedup can be achieved simply by adding modules to the implementation. It is shown that optimization criteria, e.g. minimum latency or maximum hardware efficiency, are met by very different architectures.

3. PROBLEM DEFINITION

In the decode-and-compare architecture, the n-bit retrieved codeword should first be decoded to extract the original k-bit tag. The extracted k-bit tag is then compared with the k-bit tag field of an incoming address to determine whether the tags are matched or not. As the retrieved codeword should go through the decoder before being compared with the incoming tag, the critical path is too long to be employed in a practical cache system designed for high-speed access. Since the decoder is one of the most complicated processing elements, in addition, the complexity overhead is not negligible.

Note that decoding is usually more complex and takes more time than encoding as it encompasses a series of error detection or syndrome calculation, and error correction.

- The critical path is too long
- Most complicated processing elements
- More complexity

4. RESEARCH METHODOLOGY

In the SA (saturate adder)-based architecture, the comparison of two code words is invoked after the incoming tag is encoded. Therefore, the critical path consists of a series of the encoding and the n-bit comparison. However, it did not consider the fact that, in practice, the ECC codeword is of a systematic form in which the data and parity parts are completely separated. As the data part of a systematic codeword is exactly the same as the incoming tag field, it is immediately available for comparison while the parity part becomes available only after the encoding is completed.

The proposed architecture grounded on the data path design is shown in Fig. 1. It contains multiple butterfly-formed weight accumulators (BWAs) proposed to improve the latency and complexity of the Hamming distance computation. The basic function of the BWA is to count the number of 1's among its input bits.
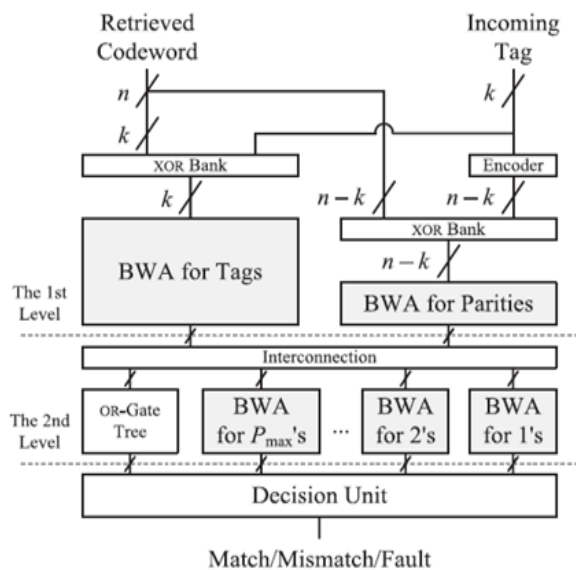
- **SYSTEM BLOCK DIAGRAM:**

Fig. 1 Proposed architecture optimized for systematic code words

5. IMPLICATION

For a set of four codes including the (31, 25) code quoted, We measured the metrics at the gate-level first and then implemented the circuits in a 0.13-μm CMOS technology to provide more realistic results by deliberating some practical factors, e.g., gate sizing and wiring delays. The latency is measured from the time when the incoming address is completely encoded. As the critical path starts from the arrival of the incoming address to a cache memory, the encoding delay must be, however, included in the latency computation. Performing post layout simulations and equivalent gate counts are measured by counting a two-input NAND as one.

The latencies of the SA-based architecture and the proposed one are dominated by SAs and HAs, respectively. As the bit-width doubles, at least one more stage of SAs or HAs needs to be added. Since the critical path of a HA consists of only one gate while that of a SA has several gates, the proposed architecture achieves lower latency than its SA-based counterpart, especially for long codewords.

The realization of this project will solve most of the difficulties discussed above and in the problem definition section. This project will have following results:
- ○ Reduce the latency
- ○ Less complexity
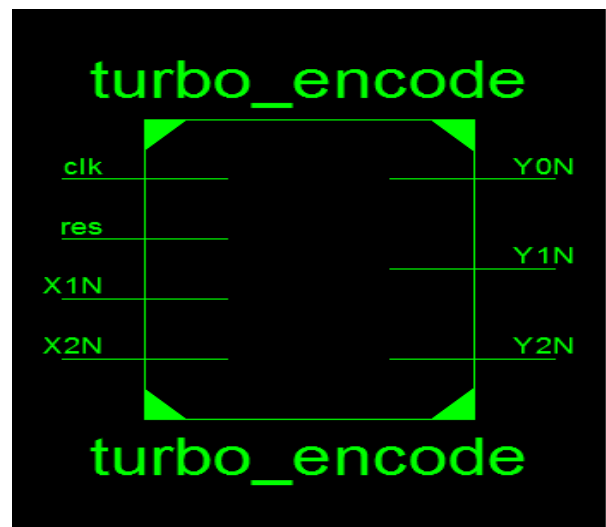- ○ High-speed access

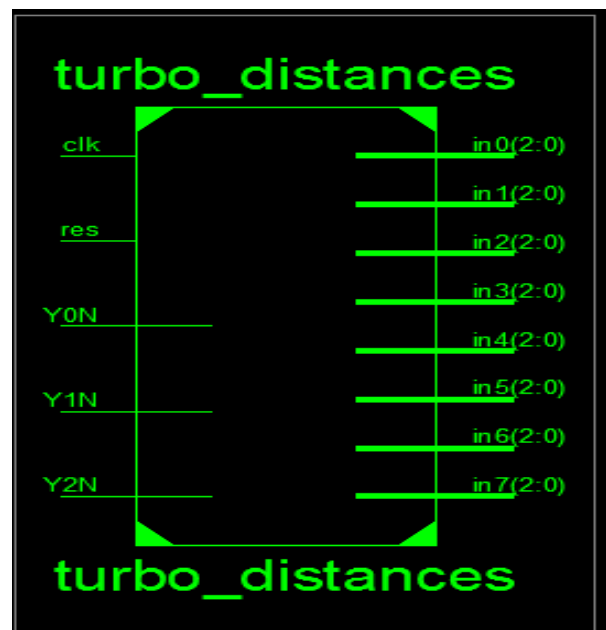- ○ Communication Decoding systems

Fig. 2 turbo distances

Fig. 3 turbo encoder

REFERENCES

[1] Susrutha Babu Sukhavasi, Suparshya Babu Sukhavasi, Dr. Habibulla Khan," Performance evaluation of turbo codes using hard decision viterbi algorithm in vhdl ,"IEEE Chiranjeevi Pilla/ International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 Vol. 2, Issue 3, May-Jun 2012

[2] Raphael Le Bidan, Camille Leroux, Christophe Jego, Patrick Adde, and Ramesh Pyndiah,"Reed-Solomon Turbo Product Codes for Optical Communications: From Code Optimization to Decoder Design," Institute TELECOM, TELECOM Bretagne, CNRS Lab-STICC, Technopˆole Brest-Iroise, CS 83818, 29238 Brest Cedex 3, France Correspondence should be addressed to Rapha¨el Le Bidan Received 31 October 2007; Accepted 22 April 2008

[3] K. Gracie is with the Communications Research Centre (CRC) Ottawa," Turbo and Turbo-Like Codes: Principles and Applications in Telecommunication," ON K2H 8S2, Canada. M.-H. Hamon is with France Telecom Research and Development, 35512 Cesson-Se´vigne´ Cedex, France Manuscript received August 24, 2006; revised December 20, 2006.

[4] Byeong Yong Kong, Jihyuck Jo, Hyewon Jeong, Mina Hwang, "Low-Complexity Low-Latency Architecture for Matching of Data Encoded With Hard Systematic Error-Correcting Codes," Manuscript received January 14, 2013; revised May 22, 2013; accepted July 25, 2013. Date of publication   August 21, 2013; date of current version June 23, 2014.IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 22, NO. 7, JULY 2014

[5] G. Fettweis and H. Meyr, "Cascaded feedforward architectures for parallel Viterbi decoding," in Proc. IEEE Int. Sym. Circuits Syst., May 1990, pp. 978–981.